UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/411,434	10/01/1999	JEAN-LOUIS TARDIEUX	TI-28234	8297

23494 7590 01/27/2003

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER
MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/411,434	TARDIEUX, JEAN-LOUIS	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- Th MAILING DATE of this communication app ars on the cover sh et with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7, 8, and 10-20* is/are rejected.

7)☒ Claim(s) *6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 5, 7, 14, 15, 16, 17, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith and Sohi, "The Microarchitecture of Superscalar Processors," IEEE, 1995 (herein referred to as Smith). Referring to claim 1, Smith has taught a digital system having a processor comprising a processor pipeline with a plurality of pipeline stages (Smith page 1609, section A. Historical Perspective, first paragraph), a plurality of protected resources connected to receive data from certain ones of the plurality of pipeline stages (Smith page 1610, section C. Elements of High Performance Processing, second paragraph) and a pipeline protection mechanism (Smith page 1614, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph), wherein the pipeline protection mechanism comprises:

a. a set of shadow registers (Smith page 1615, third full paragraph);

b. interlock circuitry for anticipating access conflicts for each protected resource of the plurality of protected resources between the pipeline stages (Smith page 1612, last paragraph in first column, continued in second column, first full paragraph in second column, and figure 2, as well as pages 1614-1615, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph) an output of the interlock detection circuitry

controllably connected to the set of shadow registers (Smith page 1615, third paragraph, particularly lines 5-13)

c. the set of shadow registers being interconnected with the processor such that a data item from a first pipeline stage can be redirected from a protected resource into a selected shadow register in response to an access conflict anticipated by the interlock circuitry so that a resource access conflict is resolved without stalling the processor pipeline (Smith page 1615, full paragraphs 1, 2, and 3).

3. Referring to claim 2, Smith has taught the interlock circuitry comprises:

a. interlock detection circuitry operable to anticipate access conflicts for all of the protected resources and operable to form a stall vector signal indicitive of anticipated access conflicts (Smith, pages 1614-1615, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph and page 1615, third full paragraph, first column, last sentence);

b. reservation and stall vector filtering circuitry connected to receive the stall vector signal and operable to select an available shadow register from the set of shadow registers in response to the stall vector signal (Smith, pages 1615, first column, third full paragraph starting at fifth line); and

c. shadow management circuitry connected to the reservation and filtering circuitry, the shadow management circuitry having an output signal controllably connected to the set of shadow registers (Smith page 1615, last full paragraph of first column and continued into second column, first full paragraph of second column, and figure 5).

4. Referring to claim 4, Smith has taught pipeline control logic for controlling the stages of the pipeline, the pipeline control logic being connected to receive the stall control signals output from the interlock circuitry based on the result of an arbitration between resources (Smith page 1615, third full paragraph, first column).

5. Referring to claim 5, Smith has taught at least one resource is selected from a group consisting of: a group of registers; a register; a field of a register; and a sub-field of a register (Smith page 1614, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph).

6. Referring to claim 7, Smith has taught the set of shadow registers is interconnected with the processor pipeline with multiplexing circuitry operable to redirect a read from a protected resource to a selected shadow register (Smith page 1615, second column, lines 7-10).

7. Referring to claim 14, Smith has taught a method of protecting a pipeline in a processor engine, wherein the processor includes a processor pipeline with a plurality of pipeline stages (Smith page 1609, section A. Historical Perspective, first paragraph) and a plurality of protected resources (Smith page 1610, section C. Elements of High Performance Processing, second paragraph), the method comprising the steps of:

a. separately arbitrating, for respective protected resources, to anticipate access conflicts between the pipeline stages for each protected resource (Smith page 1612, last paragraph in first column, continued in second column, first full paragraph in second column, and figure 2, as well as pages 1614-1615, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph), and

b. redirecting a data item from a first pipeline stage from a protected resource into a selected shadow register in response to an anticipated access conflict so that a resource

access conflict is resolved without stalling the processor pipeline (Smith page 1615, full paragraphs 1, 2, and 3).

8. Referring to claim 15, Smith has taught the method further comprising the step of selectively stalling stages of the pipeline depending upon the result of the arbitration for the respective resources to avoid resource access conflicts if the shadow register is not available to resolve an anticipated access conflict (Smith page 1615, first column, third full paragraph).

9. Referring to claim 16, Smith has taught the method of Claim 15, further comprising the step of selecting the shadow register from a plurality of shadow registers (page 1615, 3rd Full paragraph, 1st column, One of the registers is selected as a rename register from the plurality of potential rename registers, i.e. Allocating a rename register.).

10. Referring to claim 17, Smith has taught he method of Claim 14, wherein the processor pipeline is updated periodically (The processor pipeline is updated every cycle when an instruction completes, Page 1618, 2nd column "Committing State"page 1612, 2nd column, 2nd full paragraph), and wherein the step of separately arbitrating is repeated for each protected resource prior to each periodic update of the processor pipeline (Page 1618, 2nd column "Committing State"page 1612, 2nd column, 2nd full paragraph , Dependency is checked every cycle for an incoming instruction.).

11. Referring to claim 19, Smith has taught he processing engine according to Claim 1, wherein the processor pipeline is operable to update periodically (The processor pipeline is updated every cycle when an instruction completes, Page 1618, 2nd column "Committing State"page 1612, 2nd column, 2nd full paragraph), and wherein the interlock circuitry is operable to anticipate access conflicts for each protected resource during each pipeline period prior to

each periodic update of the processor pipeline (Page 1618, 2nd column "Committing State"page 1612, 2nd column, 2nd full paragraph, Dependency is checked every cycle for an incoming instruction.).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3, 8, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith and Sohi, "The Microarchitecture of Superscalar Processors," IEEE, 1995 (herein referred to as Smith) in view of Nelson et al., Digital Logic Circuit Analysis & Design, 1995 (herein referred to as Nelson). Referring to claims 3 and 8, Smith has taught interlock circuitry comprises arbitration circuitry for each protected resource (Smith page 1612, last paragraph in first column, continued in second column, first full paragraph in second column, and figure 2, as well as pages 1614-1615, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph). Smith has not taught each arbitration circuit definable as a specific form of a single, generic arbitration function. Nelson has taught the use of a generic logic function to create smaller, more specific forms of such logic (Nelson pages 173-187), such that each resource only requires enough logic to determine if there will be contention for that particular register. This would have allowed minimal use of logic as opposed to utilizing all possible logic to determine if any resource conflict has occurred (Nelson page 173, second paragraph). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to

use the method of Nelson to create each arbitration logic as a specific form of a single, generic arbitration function.

14. Referring to claim 10, Smith has taught pipeline control logic for controlling the stages of the pipeline, the pipeline control logic being connected to receive stall control signals output from the interlock circuitry based on the result of arbitration between resources (Smith page 1615, third full paragraph, first column).

15. Referring to claim 11, Smith has taught the set of shadow registers is interconnected with the processor pipeline with multiplexing circuitry operable to redirect a read from a protected resource to a selected shadow register (Smith page 1615, second column, lines 7-10).

16. Referring to claim 12, Smith has taught at least one resource is selected from a group consisting of: a group of registers; a register; a field of a register; and a sub-field of a register (Smith page 1614, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph).

17. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith and Sohi, "The Microarchitecture of Superscalar Processors," IEEE, 1995 (herein referred to as Smith) in view of Burke et al., U.S. Patent Number 5,333,176 (herein referred to as Burke). Smith has taught each of the limitations of claim 1 from which claim 13 depends. However, Smith has not taught the digital system being a cellular telephone, further comprising an integrated keyboard connected to the processor via a keyboard adapter; a display, connected to the processor via a display adapter; radio frequency (RF) circuitry connected to the processor; nor an aerial connected to the RF circuitry. Burke has taught a the digital system being a cellular telephone, further comprising an integrated keyboard connected to the processor via a keyboard adapter (figure 1, element 11 and figure 3, element 130); a display, connected to the processor via a

display adapter (figure 1, element 12 and figure 3, 124)); radio frequency (RF) circuitry connected to the processor (column 5, lines 6-14 and figure 6); and an aerial connected to the RF circuitry (figure 1). Cell phones need ever more CPU power, and Smith provides more CPU power than the CPU in the cellular telephone of Burke. It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the processor within the cellular telephone of Burke with the Superscalar microprocessor of Smith in order to provide more CPU power in the cellular telephone of Burke.

18. Claims 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith and Sohi, "The Microarchitecture of Superscalar Processors," IEEE, 1995 in view of Liptay US Patent 4,287,561.

19. Referring to claim 18, Smith has taught the method of Claim 17, wherein certain of the plurality of pipeline stages are subject to access conflicts (All of the stages are subject to access conflicts.). Smith has not specifically taught wherein the step of separately arbitrating is performed in response to resource access signals provided by each pipeline stage that is subject to access conflicts, whereby additional control storage circuitry is not required for storing conflict control information. However, Liptay has taught the step of separately arbitrating is performed in response to resource access signals provided by each pipeline stage that is subject to access conflicts (column 2, lines 48-64, each queue is subject to access conflicts, the compare logic selectively arbitrates in response to resource access signals provided from each queue), whereby additional control storage circuitry is not required for storing conflict control information. (column 2, lines 48-64, Liptay has taught that there are separate Queues that produce control dependency signals and that there is no need for additional control storage

circuitry for storing conflict control information.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Smith include the step of separately arbitrating is performed in response to resource access signals provided by each pipeline stage that is subject to access conflicts, whereby additional control storage circuitry is not required for storing conflict control information, as taught by Liplay for the desirable purpose of not having redundant dependency control information stored in an additional control storage circuitry.

20. Claim 20 does not recite limitations above the claimed invention set forth in claim 18 and is therefore rejected for the same reasons set forth in the rejection of claim 18 above.

Response to Arguments

21. Applicant's arguments filed November 13, 2002 have been fully considered but they are not persuasive.

22. On page 11 Applicant argues with regard to claim 1 in essence:

> *"Smith does not suggest anticipating a particular conflict and redirecting a particular data item to a shadow register, but instead teaches that every data transfer is sent to a temporary location, regardless of whether a conflict was present or not. Applicant's novel approach overcomes the complexity of keeping track of all data writes inherent in Smith's approach."*

However, Applicant has not claimed anticipating any particular conflict, but rather Applicant has claimed "interlock circuitry for anticipating access conflicts for each protected resource of the plurality of protected resources between the pipeline stages... ." The interlock circuitry of Smith anticipates all potential resource conflicts with respect to the architectural registers (Smith page 1612, last paragraph in first column, continued in second column, first full paragraph in second column, and figure 2, as well as pages

1614-1615, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph) and accordingly a data item is redirected from a protected resource, or architectural register, into a selected shadow register, or rename register, in response to an access conflict anticipated by the interlock circuitry so that all potential resource conflicts are resolved without stalling the processor pipeline. (Smith page 1615, full paragraphs 1, 2, and 3) Therefore Smith reads on the claimed invention.

23. On page 11 Applicant argues in essence:

"Claim 2 recites: "interlock detection circuitry operable to anticipate access conflicts for all of the protected resources and operable to form a stall vector signal indicative of anticipated access conflicts" (as amended). Smith does not detect conflicts; therefore Smith does not suggest forming such a vector."

Smith has in fact taught interlock detection circuitry operable to anticipate access conflicts for all of the protected resources by using rename registers. Furthermore, Smith has in fact taught a stall vector signal indicative of anticipated access conflicts that temporarily halts instruction dispatch if the free list of rename registers is empty. When a register cannot be renamed due to the free list being empty, the stall vector signal indicates that access conflicts may occur and the pipeline must be stalled accordingly, therefore the stall vector signal is indicative of anticipated access conflicts. (Smith, pages 1614-1615, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph and page 1615, third full paragraph, first column, last sentence)

24. On page 11 Applicant argues in essence:

"Applicant finds no teaching or suggestion in Smith of "Arbitration of resources." Smith teaches use of a mapping table to rename registers, but this is completely from arbitration. (Smith, page 1615, 3rd paragraph)"

However, as claimed, the claims do not limit the arbitration of resources to not using a mapping table to rename registers. The mapping table of Smith arbitrates, or decides which architectural registers need renaming and decides which register from the free list of rename registers to use.

25. On page 12 Applicant argues with regard to claims 3 and 9 in essence:

"Applicant agrees that Nelson does teach logic reduction; however, any sort of logic reduction applied to Smith using Nelson techniques does not result in the novel arbitration and filter schemes claimed by the Applicant."

However, Nelson is cited for the concept of using a generic logic function to create smaller, more specific forms of such logic in order to simplify the logic required (Nelson pages 173-187), such that each resource only requires enough logic to determine if there will be contention for that particular register. This would have allowed minimal use of logic as opposed to utilizing all possible logic to determine if any resource conflict has occurred (Nelson page 173, second paragraph). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the concept of Nelson in the invention of Smith to create each arbitration logic as a specific form of a single, generic arbitration function. By combining the concepts of Nelson with Smith, Applicant's claimed invention results.

26. On page 12 Applicant argues in essence:

"Referring to claim 10, as amended, Since Smith has not suggested any sort of resource arbitration, Smith does not suggest "pipeline control logic being connected to receive stall control signals output from the interlock circuitry based upon a result of arbitration between resources" as recited in claim 10."

However, since Smith has in fact taught resource arbitration (Smith page 1615, third full paragraph, first column) this argument is moot. Furthermore, Smith has in fact taught

"pipeline control logic being connected to receive stall control signals output from the interlock circuitry based upon a result of arbitration between resources" (Smith page 1615, third full paragraph, first column).

Allowable Subject Matter

27. Claims 6 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

tlm
January 23, 2003